IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 7,646,831	)	Serial No. 09/981,795
	)	
Inventor(s): Markus SCHETELIG, et al.	)	Filed: October 19, 2001
	)	
Issue Date: January 12, 2010	)	Attorney Docket No. 006916.00007

For: METHOD AND A DEVICE FOR CONTROLLING DATA EXTRACTION FROM A DATA STREAM CONTAINING AT LEAST ONE DATA PACKET

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
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Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. A copy of PTO Form 1050 is appended. The complete Certificate of Correction involves 1 page.

The mistake identified in the appended Form occurred through no fault of the Applicants, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience is the Specification filed October 19, 2001.

Issuance of the Certificate of Correction containing the correction is respectfully requested. Since this change is necessitated through no fault of the Applicants, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: April 23, 2010   By: /Kenneth Smolik/
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.:   7,646,831

DATED: January 12, 2010

INVENTOR(S):   Markus SCHETELIG. et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Title,
Please delete "Lease" and insert --Least--

Mailing Address of Sender:

Banner & Witcoff Ltd.
1100 13th Street N.W., Suite 1200
Washington DC 20005-4051

U.S. PAT. NO. 7,646,831

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FORM PTO 1050 (Rev.2-93)

Please type a plus sign (+) inside this box →   +

PTO/SB/05 (03-01)
Approved for use through 10/31/2002. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	1117.40738X00
	First Inventor	SCHETELIG, MARKUS
	Title	A METHOD AND A DEVICE FOR CONTROLLING DATA EXTRACTION FROM A DATA STREAM CONTAINING AT LEAST ONE DATA PACKET
	Express Mail Label No.	

APPLICATION ELEMENTS

SEE MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)

2. ☐ Applicant claims small entity status.
See 37 CFR 1.27

3. ☒ Specification   [Total Pages: 19]
(preferred arrangement set forth below)
-Descriptive title of the invention
-Cross Reference to Related Applications
-Statement Regarding Fed. sponsored R & D
-Reference to sequence listing, a table,
or a computer program listing appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings (if filed)
-Detailed Description
-Claim(s)
-Abstract of the Disclosure

4. ☒ Drawings (35 U.S.C. 113)   [Total Pages 3]

5. Oath or Declaration   [Total Pages ____]
a. ☐ Newly executed (original or copy)
b. ☐ Copy from a prior application (37 CFR 1.63 (d))
(for continuation/divisional with Box 18 completed)
i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s)
Named in the prior application, see 37 CFR
1.63(d)(2) and 1.33(b).

6. ☐ Application Data Sheet. See 37 CFR 1.76

7. ☐ CD-ROM or CD-R in duplicate, large table or a Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
a. ☐ Computer Readable Form (CRF)
b. Specification Sequence Listing on:
i. ☐ CD-ROM or CD-R (2 copies); or
ii. ☐ paper
c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers (cover sheet & documents(s))
10. ☐ 37 CFR 3.73(b) Statement   ☐ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document (if applicable)
12. ☒ Information Disclosure   ☐ Copies of IDS Citations
Statement (IDS)/PTO-1449
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐ Nonpublication Request under 35 U.S.C. 122
(b)(2)(B)(i). Applicant must attach form PTO/SB/35
or its equivalent.
17. ☒ Other Figs. 1-5, Credit Card Payment Form

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:

☐ Continuation   ☐ Divisional   ☐ Continuation-in-part (CIP)   of prior application No.: _____

Prior application information: Examiner: _____   Group Art Unit: _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 6b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☒ Customer Number or Bar Code Label | 022457 | or ☐ Correspondence address below
(Insert Customer No. or Attach bar code label here)

Name	ANTONELLI, TERRY, STOUT & KRAUS, LLP
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Name	Carl J. Brundidge	Registration No. (Attorney/Agent)	29,621
Signature		Date	October 19, 2001

PTO/SB/17 (10-01)
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FEE TRANSMITTAL

for FY 2002

Patent fees are subject to annual revision.

Complete if Known	
Application Number	
Filing Date	October 19, 2001
First Named Inventor	SCHETELIG, MARKUS
Examiner Name	
Group Art Unit	
Attorney Docket No.	1117.40738X00

TOTAL AMOUNT OF PAYMENT	($) 740.00

METHOD OF PAYMENT

1. ☐ The Commissioner is hereby authorized to charge indicated
   fees and credit overpayments to:
   Deposit Account Number 01-2135
   Deposit Account Name Antonelli, Terry, Stout & Kraus, LLP
   ☒ Charge Any Additional Fees Required
   Under 37 CFR 1 1 6 and 1 17
   ☐ Applicant claims small entity status
   See 37 CFR 1.27

2. ☐ Payment Enclosed:
   ☐ Check ☐ Credit Card ☐ Money Order ☐ Other

FEE CALCULATION

2. BASIC FILING FEE

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	740.00
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1)

1. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims 11 -20**	= 0	x	18	= 0
Indep. Claims 1 -3**	= 0	x	84	= 0
Multiple Dependent			280	= 0

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 0.00

**or number previously paid, if greater; For Reissues, see above.

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Fee ($)	Small Entity Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge – late filing fee or oath	
127	50	227	25	Surcharge – late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification.	
147	2,520	147	2,520	For filing a request for ex parte reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examination action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	450	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	740	246	370	For each additional invention to be examined (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify)_____

*Reduced by Basic Filing Fee Paid   SUBTOTAL (3) ($) 0.00

SUBMITTED BY

		Complete (if applicable)		
Name (Print/Type)	Carl I. Brundidge	Registration No. (Attorney/Agent)	29,621	Telephone 703-312-6600
Signature				Date 10/19/2001

A method and a device for controlling data extraction from a

data stream containing at least one data packet

1   **DESCRIPTION**

The present invention relates to a method and a device for data extraction
from a data stream containing at least one data packet, in particular for use
5   in a receiver of a wireless digital communication system.

                          BACKGROUND OF THE INVENTION

E. g. in TDMA based wireless digital communication systems, like Bluetooth,
10   data is transmitted over an air interface in separate packets with well-defined
structure. I. e. data is transmitted in a data stream containing a plurality of
data packets. Before a receiver can extract the wanted data out of these pack-
ets it has to perform different processing steps.

15   Signal parameters have to be estimated and appropriate compensation for
them has to be done. A synchronization unit, that will be described below, is
responsible for the initialization and data extraction in a Bluetooth receiver.

Bluetooth is a global standard for wireless, short-range, low-power, low-cost
20   data communication. On the physical layer a binary, gaussian shaped fre-
quency modulation with low modulation index is used.

Figure 1 shows an example of the receiving chain of a wireless TDMA receiver.
After down-conversion of the carrier frequency to an intermediate frequency
25   IF by a mixer 10, channel selection is done with a channel filter 11. Then af-
ter demodulating the waveform in a demodulator 12, the waveform (shown in
figure 2 (a) as wavy line W) is transferred into a digital representation (shown
in figure 2 (a) as X-es DW) by an AD converter 13. As a consequence a syn-
chronization unit 14, that receives the digital representation of the received
30   waveform, i. e. the digitized demodulated waveform of the received signal at
its input, can be fully digital. At its output, that is connected to a link con-
troller 15, it provides the extracted bits of the received data packets for
further processing on higher layers.

35   In order to enable data extraction different tasks have to be performed by the
synchronization unit 14.

1   The bits of a data packet are transmitted over an air interface 9 that is repre-
     sented by an antenna in figure 1, in a sequence of binary FM-modulated sym-
     bols. Thus, each symbol represents a received bit. After the FM-demodulation
     the synchronization unit 14 has to process these symbols as the symbols arri-
5   ve at the synchronization unit 14 with an unknown timing and unknown DC
     level.

     However, for data extraction unknown parameters have to be estimated. The
     DC level resulting from TX and LO offsets as well as from demodulator 12 de-
10   viations can be a few times amplitude of the waveform itself. Under cer-
     tain conditions, for example the first connection setup, the timing is totally
     unknown. For successive packets there is at least a timing uncertainty of
     ± 10 symbols.

15   Before data extraction can be started an appropriate initialization for the
     applied algorithms is required.

     First of all the presence of a packet has to be detected. When a packet has
     been detected, the accurate symbol timing needs to be determined. Also a DC
20   estimate needs to be available when data extraction starts.

     Data extraction requires that for each symbol a 1/0 or a bit decision is made,
     i.e., it has to be decided whether a symbol represents 1 or 0. Common method
     for this decision is to slice the waveform i.e. the sequence of symbols with a
25   DC estimate (shown as line DC in figure 2 (a)) into decided but oversampled
     bits illustrated in figure 2 (b). That is, based on the DC estimate for each of
     the samples within one symbol a separate bit decision is made. Then for each
     symbol one sample out of the oversampled bit stream is taken as the result of
     the actual 1/0 decision. For an optimum bit error rate performance under no-
30   isy conditions the samples corresponding to the symbol phase with optimum
     signal to noise ratio (S/N) (- the so called golden samples -) have to be taken.
     Figure 2 (c) shows the golden samples taken from the oversampled bit stream
     by appropriate sampling and the corresponding bits.

35   A DC estimate can be obtained by freezing the output of a low pass filter at an
     appropriate time instant when a packet has been detected. The position of a

1   golden sample is assumed to be in the symbol center and therefore can be di-
     rectly derived from the symbol timing.

     When data extraction has been started DC estimate and symbol timing esti-
5   mate may be continuously corrected.

     Further, in some known solutions a synchronization unit processes only al-
     ready sliced bits, i.e. it receives the oversampled bit stream. In this case, DC
     estimation is done on the radio frequency RF side. However, different DC esti-
10   mation methods (fast and slow adapting low pass filters) should be used for
     packet search and data extraction due to different performance requirements.
     Bit slicing after a false alarm (with a slow adapting low pass filter) is not ne-
     cessarily correct and a valid packet may be missed therefore.

15   Consequently, receivers have to perform a tradeoff between the packet loss
     rate (packet not recognized) and the false alarm probability (erronous indica-
     tion of a packet). Some receivers simply switch from an unsynchronous scan-
     ning mode into a synchronous mode in case a packet has been detected. In
     case of a false alarm the detection of a valid packet is often blocked then until
20   the false alarm is recognized on higher layers.

                          SUMMARY OF THE INVENTION

     Thus, the object underlying the present invention is to provide a method and
25   a device for data extraction from a data stream containing at least one data
     packet that prevents data extraction from being blocked by false alarms.

     According to the invention a method for data extraction from a data stream
     containing at least one data packet, comprises the steps of: comparing a bit
30   stream derived from a received digital data stream with an expected bit se-
     quence to determine a correlation value for detecting a data packet, starting
     data extraction when the correlation value exceeds a threshold value indicat-
     ing that a data packet has been detected, continuing comparing the received
     bit stream with the expected bit sequence to determine a new correlation
35   value, and restarting data extraction when the new correlation value exceeds
     the former correlation value.

The present invention makes it possible to highly improve data reception because the threshold value for the correlation value that is used to detect the data packet can be set relatively low, so that the packet loss rate can be kept so low that nearly no data packet is lost whereas false alarm doesn't lead to receiving invalid data. In case that a data packet is erroneously detected while no valid data packet exists, a valid data packet will not be lost, since the data packet detection is continuously performed. Thus, in case it is indicated that a data packet is received that is more likely a valid data packet since the correlation value is greater than that of the first data packet, data extraction is restarted. Therefore, a valid data packet will not be missed even if data extraction has already been started due to a false alarm.

To increase the reliability of data extraction according to the present invention the threshold value is a programmable value. Therefore, the threshold value can be adapted to different operational conditions.

To simplify the decision whether a valid data packet has been detected after starting data extraction due to a prior data packet detection, it is provided that the correlation value is stored as a correlation value each time data extraction is started or restarted and the new correlation value continuously determined after starting or restarting data extraction is compared with the actually stored correlation value.

According to an advantageous refinement of the present invention data extracted prior to restarting data extraction is rejected, because data extracted before restart is apparently false data processed due to an earlier false alarm.

To further improve data extraction an initial timing estimate is determined after detecting a data packet but prior to starting data extraction that synchronizes sampling of bits from a data stream for data extraction with data stream symbols. The instant when a packet is detected is only a rough timing information and the initial timing estimate further improves data extraction.

According to a preferred embodiment of the present invention, the timing of the sample process is continuously tracked by comparing the timing of symbols within the oversampled bitstream with the actual timing of the sample process and correcting the timing of the sample process if the deviation

1   between the timing of the sample process and the timing of symbols exceeds a
     certain value.

5   According to another aspect of the invention the method for data extraction
     from a data stream containing at least one data packet is preferably per-
     formed by a device that comprises a data extraction unit for extracting data
     from a received data stream, a packet detector for comparing a bit stream de-
     rived from a received digital data stream with an expected bit sequence to de-
     termine a correlation value, and a sync-control module receiving the correla-
10   tion value from the packet detector that controls the data extraction unit for
     starting data extraction when the correlation value exceeds a threshold value.

     Due to the packet detector that can be operated independently from the data
     extraction unit, it is possible to continuously perform packet detection even if
15   data extraction has already been started. Therefore it is possible to restart
     data extraction as required by the inventive method immediately when a new
     threshold value indicates that a data packet has been detected again, now
     with higher reliability.

20   The device further comprises an initial timing estimator which receives the
     data stream for determining an initial timing estimate prior to starting data
     extraction for synchronizing data extraction with data stream symbols, the
     initial timing estimate is output to the sync-control module.

25   The data extraction unit comprises a DC estimator deriving a DC estimate
     from the received data stream, a comparator for performing a bit decision on
     the data of the received data stream to derive an oversampled bit stream, the
     comparator has first and second inputs for receiving the DC estimate from the
     DC estimator and the data stream, respectively, and a sample-and-hold mod-
30   ule for sampling the oversampled bit stream received from the comparator.

     The data extraction unit further comprises a timing estimator receiving the
     oversampled bit stream output by the comparator for tracking the initial tim-
     ing and for controlling the sample-and-hold module.

35
     Since the data extraction unit comprises a timing estimator for continuously
     tracking the timing or synchronization it is possible that the initial timing es-

1   timator can work in the same way as before after starting data extraction, so that in case that a further data packet has been detected with higher reliability restarting data extraction can be performed in the same way as starting data extraction at the first time.

5

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be explained in more detail hereinafter with reference to the accompanying drawings showing preferred embodiments.

10

Figure 1 shows a simplified block diagram of the receiving chain of a conventional tranceiver used for wireless communication.

Figure 2 shows different diagrams for (a) the demodulated waveform, the digi-
15   talized demodulated waveform and the DC level, (b) the oversampled bit stream and (c) the extracted bit data stream with the respective bits.

Figure 3, a simplified schematic block diagram of a device according to the present invention that can be used as synchronization unit.

20

Figure 4, a simplified schematic diagram of a sync-control state machine used with the present invention.

Figure 5, a simplified schematic block diagram of a timing estimator used in
25   a data extraction unit of a synchronization unit according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

30   The device for data extraction, e.g. a synchronization unit, according to the present invention is realized with a highly modular structure. As can be seen in Figure 3 the main parts of the synchronization unit are a preprocessing module 16 that might contain ADC postprocessing or postdetection filtering of the demodulated signal, a packet detector 17 that scans the input signal, i.e.
35   the digital representation of the demodulated waveform for valid access codes, an initial timing estimator 18 that provides an initial estimate of the symbol timing, a DC estimator 19 that generates initial as well as continuously

1   tracked DC estimates for symbol slicing, a comparator 20 for symbol slicing, a
      timing estimator 21 for continuously tracking the symbol timing, a sample-
      and-hold   module 22 that performs the downsampling, and a sync-control
      module 23 that controls all modules given above.

5
      In general, the preprocessing module 16 might contain ADC postprocessing or
      postdetection filtering of the demodulated signal.

      E. g., the preprocessing module 16 is responsible for postdetection low pass
10   filtering is used for optimizing the bit error rate under noisy and interfering
      conditions. Output is the low pass filtered digital waveform representation
      DW of the demodulated waveform W. The preprocessing module 16 is placed
      at the radio frequency/baseband (RF/BB) interface.

15   The packet detector 17 is responsible for indicating the presence of valid pa-
      ckets. The packet detector 17 gets the demodulated and filtered waveform sig-
      nal DW as input and provides a correlation value CorrVal as output signal.
      The correlation value CorrVal indicates the degree of similarity between the
      bit sequence of the received waveform and an expected bit sequence.

20
      A packet detector 17 for TDMA transceivers that can be used with the present
      invention is described in detail in the copending U.S. patent application (At-
      torney's Docket No ...) filed on the same day as the present application and
      claiming the priority of the German patent application DE 100 51 889, the
25   disclosure of which is incorporated in this specification by reference. In this
      application the calculation or the estimation of the correlation value is ex-
      plained.

      The initial timing estimator 18 also processes the digital demodulated wave-
30   form signal DW. During a given search time, indicated by the sync-control
      module 23, the initial timing estimator 18 determines the accurate symbol ti-
      ming. The initial symbol timing estimate is delivered to the sync-control mod-
      ule 23.

35   The DC estimator 19 performs two tasks. Again the digital demodulated wave-
      form signal is processed. By selecting an appropriate sample of an internal
      low pass filter an initial DC estimate is generated. Afterwards this DC estima-

1   te is continuously tracked i.e. in case of a DC drift resulting from a carrier frequency drift the DC estimate is continuously corrected. The DC estimate is supplied to the comparator 20 for symbol slicing.

5   The comparator 20 simply compares the digital waveform signal DW with the DC estimate and performs the symbol slicing by providing the value 1 in case that the value of the waveform signal DW is greater than the DC estimate or the value 0 in case that the value of the waveform signal DW is less than the DC estimate. Therefore, the output of the comparator 20 is an oversampled
10 stream of bits as shown in figure 2b.

    The timing estimator 21 continuously tracks the symbol timing estimate. It starts with an initial timing estimate that it gets from the sync-control module 23. The timing estimator 21 evaluates the edges of the demodulated wave-
15 form which are internally generated by processing the oversampled bit stream received from the comparator 20 and compares estimated timing and actual timing of the edges. The actual timing may be equal, early or late compared to the estimated timing. In case there is a certain tendency towards either early or late, the estimated timing is corrected appropriately. The symbol timing es-
20 timate STE is provided to the sample-and-hold module 22 as output signal of the timing estimator 21. The symbol timing estimate STE can be actually formed by two signals, wherein the timing information is indirectly coded on them.

25 The sample-and-hold module 22 performs the downsampling by taking out the golden samples for the symbol decision. The sample-and-hold module 22 also provides the interface to the following circuits (not shown) which further process the extracted data on higher layers. Besides the extracted data B it-self, a signal for indicating the data start (FrameSync) is needed also.
30
    The sync-control module 23 controls the synchronization process. It is based on a state machine where the states correspond to the different phases of the synchronization process. With the SyncWin signal higher layers can indicate to the sync-control module 23 when a valid packet has to be expected. The
35 output of the sync-control module 23 is the current state of the internal sta-te machine. With the SyncWin signal the other modules of the synchronizati-on unit are controlled.

1   A detailed description of the synchronization unit focussing on the sync-control state machine and the timing estimation will now be given with reference to figure 4.

5   The synchronization process can be split into different phases. These phases are represented by different states of the state machine inside the sync-control module 23. These phases are:

INIT: All modules are initialized to a well-defined startup sta-
10 te.
SEARCH PACKET: A valid packet is searched.
PACKET FOUND: A valid packet has been found.
SEARCH TIMING: The accurate symbol timing is searched.
SYNCFOUND: The symbol timing, i.e. synchronization, has been found.
15 ACTIVE: Data extraction is running, however the search for valid packets is still continued.
FINISHED: Data extraction is running until the synchronization unit is switched off, no packet search is done anymore.

20   When the synchronization unit is switched on, i. e. the clock is running but a signal enable is low, i. e. the signal enable equals 0, the state INIT is entered. Internal registers are reset to default or programmable values. The state INIT is left and the state SEARCH PACKET is entered when the enable signal is set to high, i. e. the enable signal equals 1.

25
By entering the state SEARCH PACKET the packet detector 17 as well as the initial timing estimator 18 are enabled. The packet detector 17 delivers a correlation value CorrVal to the sync-control module 23 which indicates the degree of similarity between a bit stream of a received demodulated waveform
30 and the expected access code or synchronization word. When CorrVal exceeds a programmable threshold CorrThres the wanted packet is supposed to be found. In this case the state PACKET FOUND is entered in case that the signal SyncWin is high or 1.

35   Always when the state PACKET FOUND is entered the latest correlation value CorrVal is stored in a register MaxCorrVal of the sync-control module 23 (not shown).

1   Whenever a new correlation value CorrVal from the packet detector 17 ex-
ceeds the registered correlation value MaxCorrVal, while at the same time the
state FINISHED has not been reached, while the signal SyncWin is high or 1
the state PACKET FOUND is reentered and MaxCorrVal is set to the new va-
5   lue. I. e., the synchronization process can be restarted in the state PACKET
FOUND. As a consequence the synchronization unit can continue with scan-
ning for access codes while data extraction is already prepared or even star-
ted. In case the correlation value CorrVal indicates a higher level of confi-
dence (higher correlation value CorrVal) compared to the last packet detec-
10   tion, the synchronization process is restarted. So far extracted data is rejec-
ted. Restarting of the synchronization process may be called multiple sync-
found.

An advantage of multiple sync-founds is that the tradeoff between the false
15   alarm rate and the packet detection performance under noisy conditions is
eased, as always the best matching sequence can be detected. False alarms
do not block the synchronization unit to detect access codes received with
sufficient signal quality. Normally false alarms do not reach the highest pos-
sible correlation value CorrVal levels
20

The state PACKET FOUND can only be entered when a signal SyncWin is set
to 1. Otherwise the result of the correlation value CorrVal evaluation is igno-
red. By means of the signal SyncWin higher layers can control the synchro-
nization process. A well-defined time window for synchronization can be given
25   as a consequence.

When the state PACKET FOUND is entered the timing of the detected packet
is already roughly known. However the inaccuracy is nearly ±1 symbol. As a
consequence the initial timing estimator 18 has to search for the accurate ti-
30   ming during one symbol period only. This allows an efficient implementation
of the initial timing estimator 18.

The state PACKET FOUND is left when the search time for the initial symbol
timing estimate starts. The search time starts a programmable time after the
35   state PACKET FOUND has been entered. A counter WinCount is started when
the state PACKET FOUND is entered. When the counter WinCount value re-
aches the programmable value WinStart the state SEARCH TIMING is entered.

1   The counter WinCount continues to run in the state SEARCH TIMING. The de-
lay given by value WinStart between packet detection and start of the initial
timing search is needed as the packet detector 17 and the initial timing esti-
mator 18 trigger on different parts of the processed access code. The packet

5   detector 17 triggers at the end of the synchronization word and the initial ti-
ming estimator 18 triggers at the end of the trailer bits of the received data
packet.

In the state SEARCH TIMING the sync-control module 23 waits for the trigger
signal InitTiming from the initial timing estimator 18. When the trigger signal

10   InitTiming arrives, i. e. when the signal InitTiming equals 1 or when the
counter WinCount reaches the programmable value WinStop the state SYNC-
FOUND is entered.

15   The state SYNCFOUND only lasts for one clock cycle. It indicates to the other
modules that an access code with the accurate symbol timing has been found,
i.e. that synchronization has been found. The timing estimator 21 and the
sample-and-hold module 22 are initialized during the state SYNCFOUND. In
these modules 21 and 22 modulo counters with a period corresponding to the

20   symbol period are started then. The state SYNCFOUND is immediately left.
Normally the state ACTIVE is entered. Except for the one condition that the
counter CorrVal value exceeds the registered value MaxCorrVal while the sig-
nal SyncWin is set. In this case the state PACKET FOUND is entered.

25   The state ACTIVE lasts for a programmable time MaxSearchTime. When it is
entered the counter AfterSFCount is started. When this counter AfterSFCount
value exceeds the programmable value MaxSearchTime the state FINISHED is
entered.

30   During the state ACTIVE as well as during the state FINISHED the data ext-
raction is active. However during the state ACTIVE the synchronization pro-
cess can be restarted under the known conditions bound to the values Corr-
Val, MaxCorrVal and SyncWin.

35   The state FINISHED is left when the synchronization unit 23 is disabled. In
this case the state INIT is entered again when the signal enable is set high.
Normally the synchronization unit 14 is switched off inbetween.

1   The synchronization unit 14 is not responsible for detecting the end of the
    user data. Higher layers have to stop the data evaluation at the appropriate
    time.

5   Advantage of the modular structure of the synchronization unit 14 according
    to the present invention is that the modules for packet detection and symbol
    timing estimation (packet detector 17, initial timing estimator 21) can conti-
    nue to work when the data extraction is already started.

10 For an optimum receiver performance in terms of bit error rate the most ap-
    propriate samples within the oversampled bit stream from symbol slicing -the
    so called golden samples- have to be used to represent the received bits.

    The task of the timing estimator 21 is to set the sample time for the sample-
15 and-hold circuit 22. After initialization the timing estimator 21 continuously
    corrects the sampling time. Main reason for the continued correction is to
    compensate for initial timing errors after synchronization. A second reason is
    to compensate for deviations between the transmitter and receiver bit clock.

20 The timing estimation is done with an edge detection procedure. That means
    that the edges of the oversampled data signal from symbol slicing are used to
    estimate the symbol timing. As the received and filtered symbols are symme-
    tric the so called golden samples are found in the center of each symbol. Due
    to the symmetry of the symbols the edges are always positioned in the center
25 between two symbols. Consequently the edges occur with a fixed phase of half
    a symbol relative to the golden samples.

    The timing estimation is done in two steps. In the first step for each edge on
    the data signal from symbol slicing, i. e. the oversampled bit stream, the esti-
30 mated timing of an expected edge is compared with the actual edge timing.
    The estimated timing of an expected edge can be generated by delaying the la-
    test sampling trigger by half a symbol. The sampling triggers correspond to
    the estimated timing of the golden samples. The estimated timing of edges
    and the estimated timing of golden samples can be regarded as certain pha-
35 ses of the estimated symbol timing.

1   If the estimated edge timing appears to be early an early-late-counter 31 va-
     lue (cf. Fig.5) is decremented. If it appears to be late the early-late-counter 31
     value is incremented. This is done for each actual edge that appears. When
     actual edges and estimated edges occur at the same time the early-late-coun-
5   ter 31 value is unchanged. Also when no actual edges occur due to a se-
     quence of equal bits the early-late-counter 31 will keep its value.

     In the second step the early-late-counter 31 value is compared to a pro-
     grammable threshold CorrectionThres. If the positive or negative value of the
10   early-late-counter exceeds this threshold CorrectionThres the estimated sym-
     bol timing is appropriately corrected. With this threshold the adaptation
     speed of the timing estimation is controlled. After correction of the estimated
     symbol timing the early-late-counter 31 value is set to 0 again. The early-
     late-counter value is also set to 0 at initialization in the state SYNCFOUND.
15
     Figure 5 shows an example for an implementation of the timing estimation in
     the timing estimator 21.

     The estimated edge timing is given with a signal ExpectedEdge that can be in-
20   ternally generated from the current symbol timing estimate, i. e. from the
     current golden sample timing estimate, by delaying the sample trigger by half
     a symbol as mentioned above. The bit stream from symbol slicing, i.e. the
     output signal of the comparator 20, is used in the timing estimator for gene-
     rating the signal ActualEdge by performing edge detection on this signal.
25
     The signal ExpectedEdge and a signal ActualEdge generated by an edge de-
     tector 24 are fed each into a tap delay line 25, 26 with a length of roughly
     half a symbol. The taps of each of the tap delay lines 25, 26 are respectively
     connected to first and second AND gates 27, 28 via respective OR gates 29,
30   30. The signal ActualEdge output by the edge detector 24 is fed to a second
     input of the second AND gate 28 the first input of which receives the output
     of the second OR gate 30 that is connected with the second tap delay line 26
     receiving the signal ExpectedEdge. Similarly, the signal ExpectedEdge is fed
     to a second input of the first AND gate 27 the first input of which receives the
35   output of the first OR gate 29 that is connected with the first tap delay line
     25 receiving the signal ActualEdge.

1   By respectively comparing each one of the signals ActualEdge and Expected-
    Edge with the delayed taps of the other it is checked if one event (i.e. expec-
    ted or actual edge) occurred before the other. If so, a corrsponding trigger
    Early or Late is respectively set and the early-late-counter 31 is appropriately
5   changed. Under normal operation ExpectedEdge and ActualEdge events occur
    at maximum only a few samples apart. In addition, ExpectedEdge and Actual-
    Edge events occur at most only once during a period of nearly one symbol.

    When the early-late-counter 31 value exceeds the correction threshold Cor-
10 rectionThres the estimated symbol timing is appropriately shifted one sample
    by incrementing or decrementing the signal SelSampleNo by correction means
    32 associated with early-late-counter 31. I. e., if early-late-counter 31 value
    is less than the negative value of the threshold CorrectionThres the signal
    SelSampleNo is incremented, whereas, when the early-late-counter 31 value
15 is greater than the positiv threshold CorrectionThres the signal SelSampleNo
    is decremented. The early-late-counter 31 value is then reset to zero again.

    The timing estimator 21 as well as the sample-and-hold circuit 22 are initiali-
    zed in the state SYNCFOUND. The state SYNCFOUND occurs with a known fi-
20 xed phase relative to the received demodulated waveform signal. SelSampleNo
    is a certain phase relative to a free running modulo counter 33 (period 1 sym-
    bol) which is initialized at the SYNCFOUND state. At initialization Sel-
    SampleNo is set to a well-defined value which represents the initially estima-
    ted timing of golden samples. As a consequence the current symbol timing es-
25 timate is given with the signal SelSampleNo.

    The symbol timing estimate STE, i.e. the estimated timing of the golden
    samples is delivered to the sample-and-hold circuit 22 with two signals, i.e.
    the signal SelSampleNo and the output of counter 33. The free running mo-
30 dulo counter 33, is used as a reference time. The modulo counter 33 is star-
    ted when the sync-control circuit 23 enters the state SYNCFOUND by a start
    signal Start. The second signal SelSampleNo determines the actual sampling
    time. When SelSampleNo and modulo counter 33 value are equal the
    sampling is triggered. When SelSampleNo is incremented by 1 the sample ti-
35 ming is delayed one sample. When SelSampleNo is decremented by 1
    sampling takes place one sample earlier.

1   Purpose of the two-signal solution instead of one sampling trigger signal is to
     deliver besides the actual timing also information about the initial timing to
     the sample-and-hold circuit 22.

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